Automated Hierarchical Floorplanning for Reconfigurable Logic

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Long compilation times are a limiting factor to the use of commodity FPGAs in a reconfigurable computing system. To speed up compile time and thus facilitate rapid application development, we present a new hierarchical floorplanner specifically designed for computing. This floorplanning methodology is applied to the base FPGA place and route problem. Our algorithms take advantage of the structured nature of FPGA-computing applications by reducing device place and route to a hierarchy of design subproblems.

Depending on the design style, integrated circuit placement has different goals. In traditional FPGA layout, the target device has a fixed amount of routing area and a placer attempts to find locations for circuit elements that ensure routability within this area. Typically, a computationally-expensive simulated annealing algorithm searches for a minimum total wire length cell configuration, optimizing for routability [2]. Following placement of each discrete array component, a router forms physical connections. Due to the combined complexity of these two NP complete problems and the large number of primitive FPGA logic elements, feedback between these two processes is rarely feasible.

In contrast to FPGA layout, the goal of general-cell placement is to position irregularly-shaped components of a circuit so that layout area is minimized [4]. This bin packing problem is concerned with placing a number of cells of variable sizes and shapes tightly into a rectangle while minimizing total interconnection wire length between the shapes. For designs with user-defined hierarchy, an iterative approach of cell shaping, relative placement, and global wiring can be used, effectively reducing the overall layout problem to a series of design subproblems. Most FPGA-computing applications contain design hierarchy in the form of bit-sliced datapath components such as adders, subtractors, ALUs, and memories. Interconnection between these macroscopic elements is constrained less by localized congestion but rather by macro shapes and relative positionings as in the general-cell placement problem. To date, FPGA place and route approaches have failed to address this regularity even as device sizes have expanded and the complexity of the overall place and route problem have lead to increasingly long compile times. To take advantage of design heirarchy, we merge general-cell floorplanning and global-routing techniques with existing FPGA layout. This approach will take advantage of circuit hierarchy globally while continuing to optimize for design routability locally.

Like other existing floorplanning systems [3] [5], design input to our system is represented as a cut-tree with multi-element macrocells at the leaves and combinations of these macrocells represented as interior nodes. As seen in Figure 1, constructing a floorplan from this representation amounts to assigning each cut-tree node geometrical and topological information. After floorplanning, each leaf macrocell is treated as an independent place-and-route problem using existing routability-based place-and-route methods subject to the size and external routing constraints determined by the floorplanning process. The overall hierarchical process may be broken into three distinct phases:

1. *Phase 1* (Floorplan Sizing): In this phase we enumerate different possible floorplan alternatives by performing a bottom-up tree traversal of the given cut-tree. At each interior node of the cut-tree we apply a shape function [6] to determine a range of minimum-area subfloorplans based on the feasible shapes of each child node. For example, a number of possible shapes for node 1 in Figure 1 are derived from the possible given shapes of its children nodes A, B, and C. At the end of this phase each node is labelled with a set of feasible minimum area shapes of varying dimensions.

2. *Phase 2* (Floorplan Construction and Global Routing): In this phase we perform a top-down cut-tree traversal starting at the root of the tree. At each level, the dimensions of possible floorplans are compared against the dimensions of a fixed target room (eg the physical dimensions of the chip for the root) so that infeasible floorplans may be eliminated from consideration. Global routing between subcircuits is used to select a sub-floorplan at this level with minimum overall wire length as well as to set pin locations for sub-floorplans at the next level of the tree. In Figure 1, the sub-floorplans

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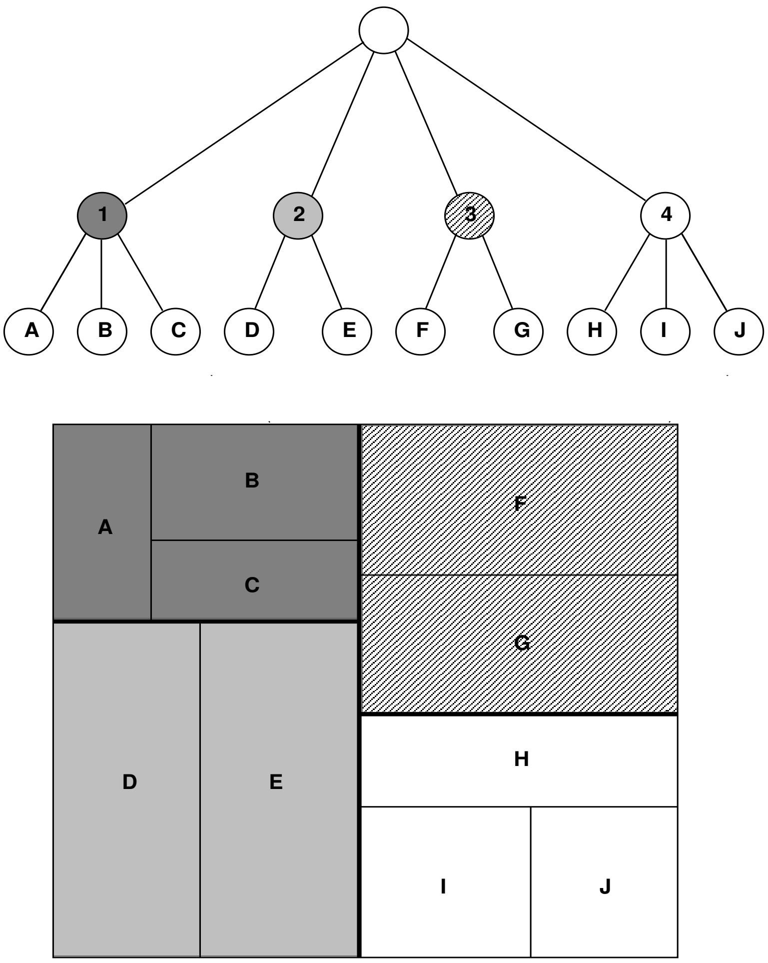

Figure 1: Floorplan Constructed from a Cut Tree

for each of the numbered nodes is reflected by shading.

3. *Phase 3* (Macrocell Synthesis) - Following the floorplanning phase, each macrocell has a specific shape with set external signal connections. Exisiting FPGA place and route approaches can be used on each macrocell individually. Due to the reduced size of each place and route problem, the combined compilation time of these tasks is considerably less than the compilation time of a design which considers all design elements simulataneously.

This approach has been implemented and is currently being tested with several FPGA computing examples including a shortest path search [1] and the generation of Mandlebrot curves.

References

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