How Does the Substrate Conductivity Affect the On-Chip Coupling Inductance Behaviour?

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Abstract

The goal of this work was to extend the FastHenry 3-D inductance extraction program[1] to include volume ground planes like semiconductor substrates, and then use the modified program to investigate a simple model for predicting on-chip inductive coupling between parallel lines. Our results demonstrate that a formula based on a simple two-loop model, accurately predicts high-frequency limit inductive coupling. However, our simulation studies show that the high-frequency limit is higher than 20 gigahertz, because of the poor conductivity of the substrate. Therefore, as a practical matter, models for coupling inductance must correctly predict the low frequency coupling inductance. Finally, we show that the simple two-loop model is inadequate, primarily because of the three-dimensional nature of the substrate current distribution.

Two-dimensional analysis[2] for two rectangular loop structure, leads to a simple formula for the coupling inductance, This formula is function of the loop length, height and separation. In order to examine whether that formula can be used to predict on-chip coupling inductance, a volume filament discretization for the semiconductor substrate was added to the FastHenry program, as shown in Figure 1. As the coupling inductance was plotted as a function of volume discretization for both very high and very low frequency, the formula based on the two-loop model accurately predicts the high frequency coupling inductance. For this comparison, the loop height was set to twice the distance to the substrate, based on the method of images approach[3].

The modified FastHenry program was also used to compute the coupling inductance as a function of frequency, for both realistic and idealized substrate conductivities. The results clearly indicated that with a semiconductor substrate, and assuming operating frequencies below 20 gigahertz, it is the low-frequency-limit inductance, not the high-frequency-limit inductance, that is most important for predicting on-chip inductive coupling.

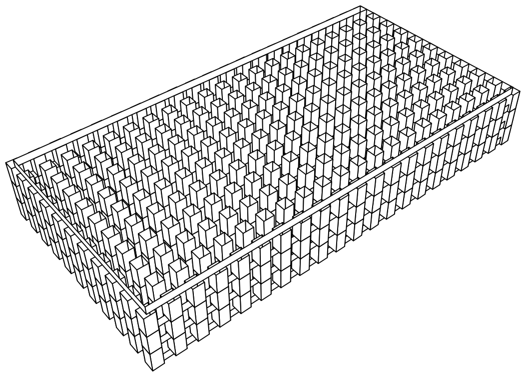

Figure 1: Volume filament-based discretization of the substrate.

The two-loop model is inadequate for modeling the low-frequency-limit inductance. It was shown that even by selecting a modified loop width, in the two-loop model, the model does not accurately predict parallel line inductive coupling over a range of conductor separations, as shown in Figure 2.

The simple model fails primarily because the low-frequency coupling inductance over a substrate ground plane is more three-dimensional in nature than can be modeled by a loop. This three-dimensional behavior is due primarily to the current spreading from the contact points through the substrate, as shown in Figure 3.

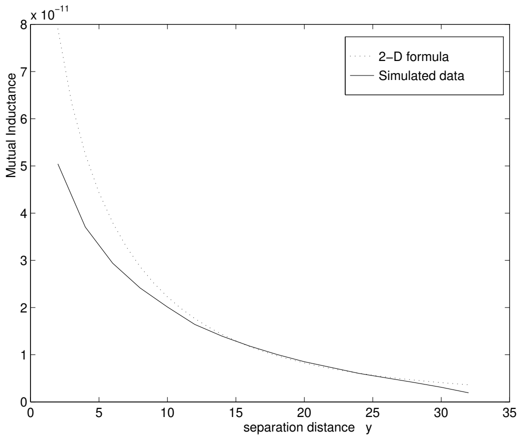

Figure 2: Comparison of the coupling inductance predicted by equation(1), and the simulated coupling inductance as a function of separation distance. Note that a “best-fit” loop height of 14.3μ was used for the comparison but the conductors are only 1μ above the ground plane.

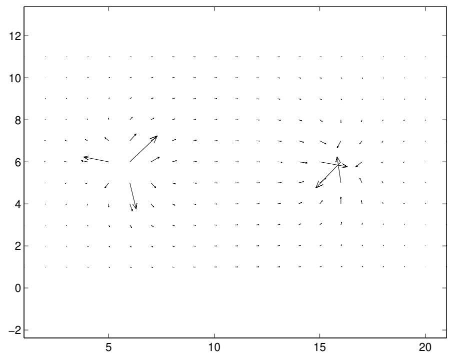

Figure 3: Substrate surface current distribution at low frequency.

References

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