NuMesh Video System Using Distributed Frame Buffers[1]

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General Overview

The NuMesh Video system consists of several VRAM boards and a DAC (digital to analog conversion) board. This *video pipeline* is connected to the NuMesh communications substrate [1] (see Figure 1). The DAC is connected to a 21" multisync RGB monitor.

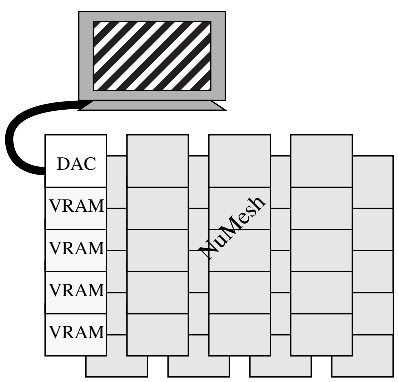

Figure 1

Each VRAM board contains a full frame buffer (1024x1024 pixels). Each pixel contains 8 bits of Zbuffer data and 24 bits of RGB data (see Figure 2). The processors connected to the NuMesh substrate can write to any of the boards whenever it wants. Each board allows NuMesh to reset the board, disable or enable reading of the buffer, set the start address for pixel writing, and write the pixel's RGB and/or zbuffer data to the buffer.

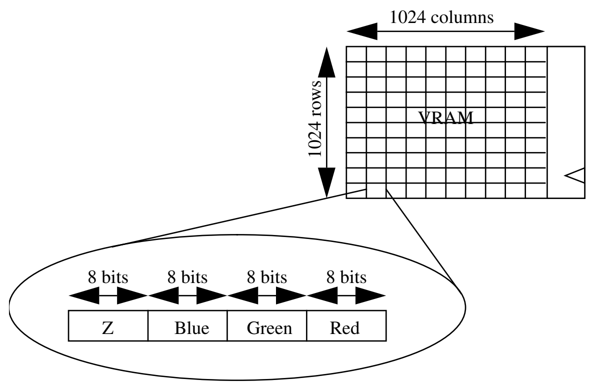

Figure 2

Video Pipeline

Whenever the DAC board needs a new row of pixels, it sends a request down the video pipeline through the VRAM board chain along with synchronizing information. The pixel request moves down the chain and then back up. The VRAM only recognizes this request as it moves up the chain back towards the DAC, upon which it sends the requested pixels up the video pipeline.

The synchronizing information is used to make sure that along the video pipeline, the correct pixel is being read in each VRAM board during every cycle. For example, if there are two VRAM boards, the board furthest from the DAC (Board 0) should read its local VRAM first. So in cycle 0 (after Board 0 is initially synchronized), Board 0 will read the pixel corresponding to location (0,0) on the screen (and also in the VRAM) and send it up the video upline. In cycle 1,

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2. Steve Ward, Frank Honore, and Russ Tessier contributed in helping to design this system.

Board 1 will read pixel (0,0) while Board 0 will read pixel (0,1).

Whenever a pixel arrives along the video pipeline into a new VRAM board, the value of its Zbuffer is compared to the Zbuffer value of the pixel being read out of the local VRAM. The pixel with the higher Zbuffer value is sent along the video pipeline to the next VRAM board and eventually to the DAC. Using our previous example, when pixel (0,0) from Board 0 arrives in Board 1 during cycle 1, its Zbuffer value is compared to pixel (0,0) from Board 1's local VRAM. The pixel with the higher Zbuffer value is sent to the next VRAM board Figure 3 illustrates the concepts of the video pipeline.

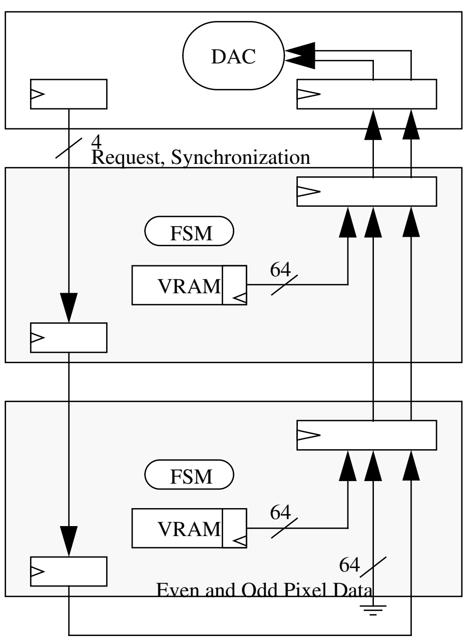

Figure 3: Video Chain

Numesh Interface

Processors connected to the NuMesh communication substrate have a great deal of flexibility and control of the video system. NuMesh can write to any of the VRAM buffers at the same time pixels are being read out of the VRAM buffer. NuMesh can control where and what it wants to write. Reading of any VRAM buffers can be disabled. Once every frame refresh cycle NuMesh receives a signal from the DAC board that vertical synchronization is occuring. This allows NuMesh to set up double buffering easily.

Conclusions and Future Work

This abstract describes a hardware project to enable exciting graphics applications to be run on the NuMesh communcations substrate. NuMesh is ideally suited to static applications that can be highly parallelized such as graphics applications.

An initial design of the VRAM board is ready to be fabricated. Most of the design work for the DAC board is near completion. We anticipate a functioning system within the next few months.

References

[1] S. Ward, K. Abdalla, R. Dujari, M. Fetterman, F. Honore, R. Jenez, P. Laffont, K. Mackenzie, C. Metcalf, M. Minsky, J. Nguyen, J. Pezaris, G. Pratt, R. Tessier. "The NuMesh: A Modular, Scalable Communication Substrate", *In Proceedings of the International Conference on Supercomputing*, July 1993